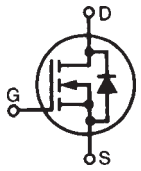
IXYS

Polar™ Power MOSFET HiPerFET™

IXFR32N100P

V_{DSS} = 1000V
I_{D25} = 18A
$R_{DS(on)}$ ≤ 340mΩ
t_{rr} ≤ 300ns

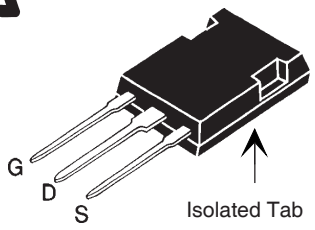
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	1000	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	1000	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	T_C = 25°C	18	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	75	A
I_{AR}	T_C = 25°C	16	A
E_{AS}	T_C = 25°C	1.5	J
dV/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	15	V/ns
P_D	T_C = 25°C	320	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	Maximum lead temperature for soldering	300	°C
T_{SOLD}	Plastic body for 10s	260	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
F_C	Mounting force	20..120/4.5..27	N/lb.
Weight		5	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0V, I_D = 3mA	1000			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 1mA	3.5		6.5	V
I_{GSS}	V_{GS} = ± 30V, V_{DS} = 0V			± 200	nA
I_{DSS}	$V_{DS} = V_{DSS}$			50	μA
	V_{GS} = 0V, T_J = 125°C			2.5	mA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 16A, Note 1			340	mΩ

ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Features

- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Low drain to tab capacitance(<30pF)
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier

Applications

- Switched-mode and resonant-mode power supplies
- DC-DC converters
- Laser Drivers
- AC and DC motor controls
- Robotics and servo controls

Advantages

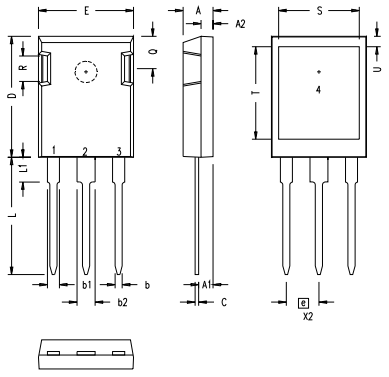
- Easy assembly
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 20V, I_D = 16A, Note 1	13	21		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		14.2		nF
C_{oss}			815		pF
C_{rss}			60		pF
R_{Gi}	Gate input resistance		1.50		Ω
$t_{d(on)}$	**Resistive Switching Times**		50		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 16A		55		ns
$t_{d(off)}$	R_G = 1Ω (External)		76		ns
t_f			43		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 16A		225		nC
Q_{gs}			85		nC
Q_{gd}			94		nC
R_{thJC}				0.39	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode (T_J = 25°C unless otherwise specified)		Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			32	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			128	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			1.5	V
t_{rr}	I_F = 16A, -di/dt = 100A/μs			300	ns
Q_{RM}	V_R = 100V, V_{GS} = 0V		2.2		μC
I_{RM}			15		A

Note 1: Pulse test, t ≤ 300μs; duty cycle, d ≤ 2%.

ISOPLUS247 (IXFR) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Fig. 1. Output Characteristics @ 25ºC

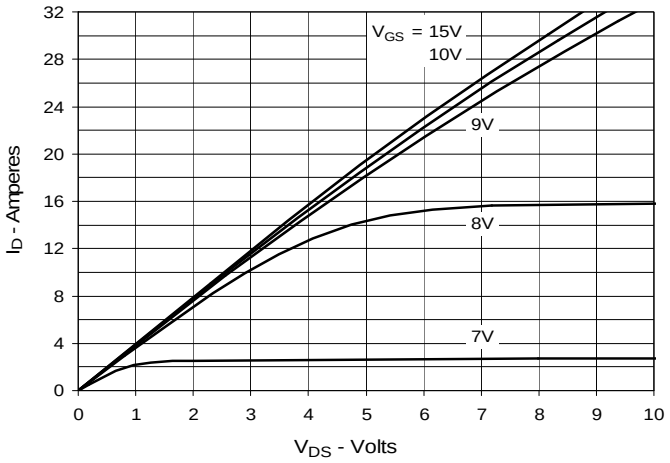


Fig. 2. Extended Output Characteristics @ 25ºC

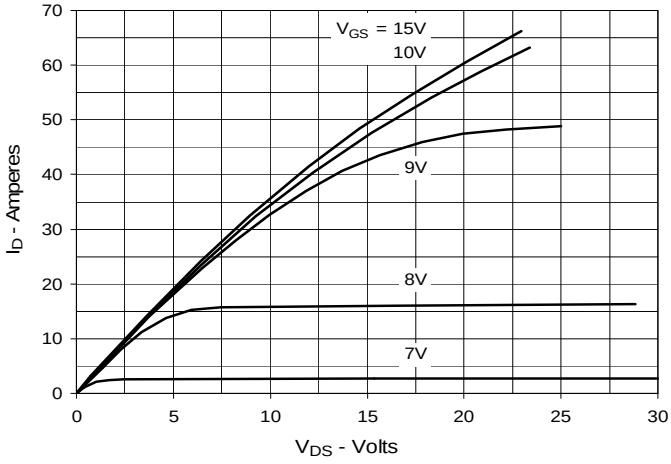


Fig. 3. Output Characteristics @ 125ºC

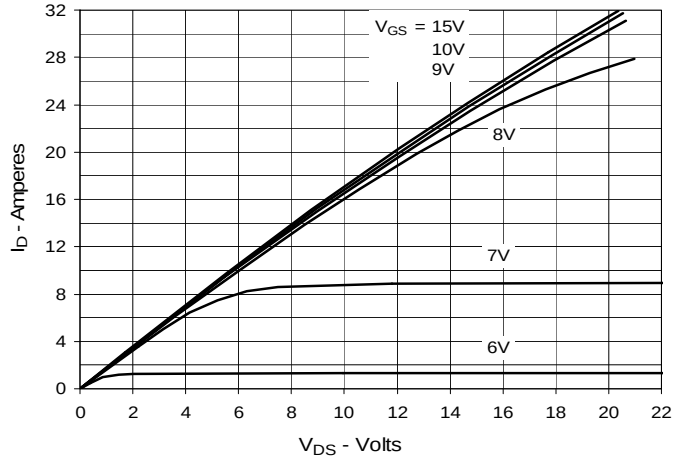


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 16A Value vs. Junction Temperature

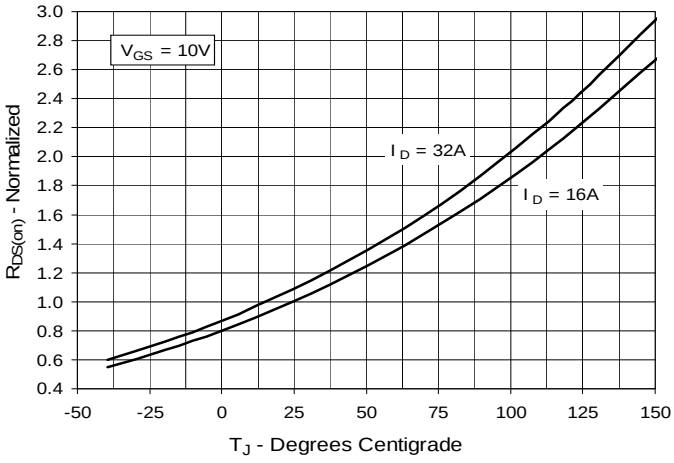


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 16A Value vs. Drain Current

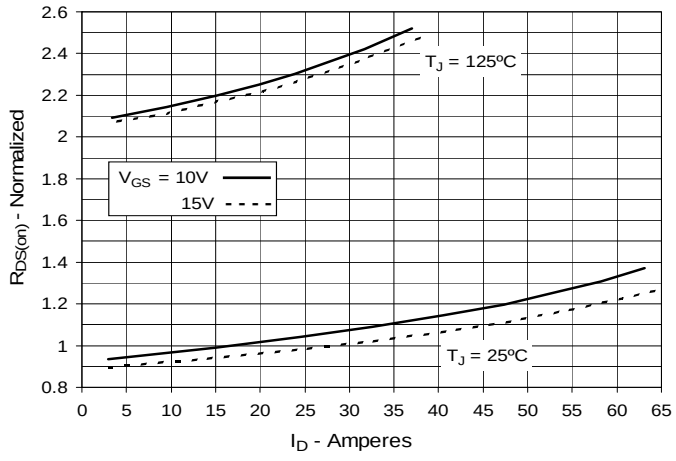


Fig. 6. Maximum Drain Current vs. Case Temperature

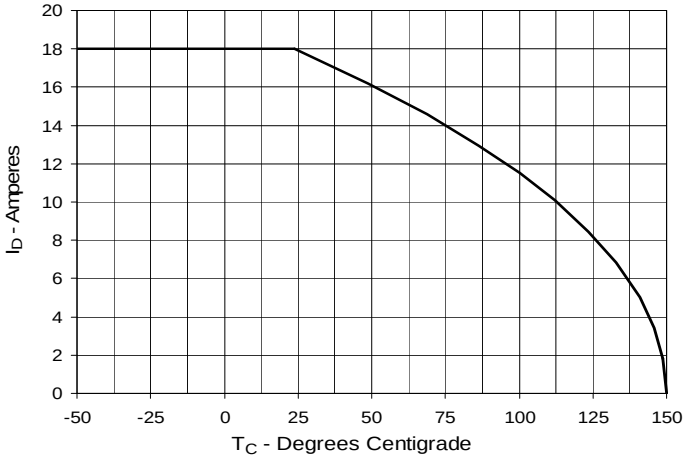


Fig. 7. Input Admittance

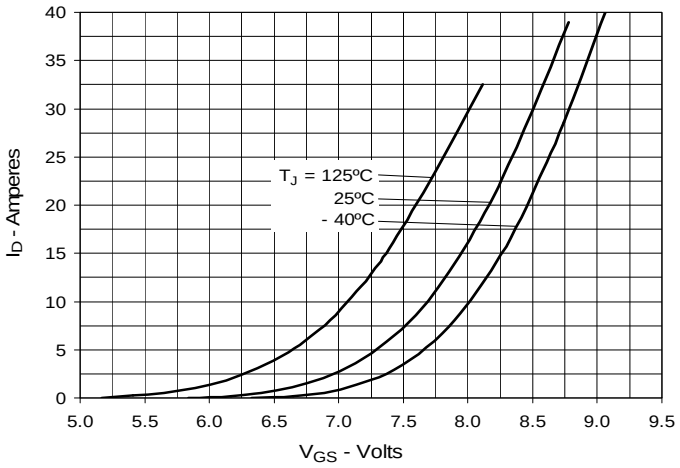


Fig. 8. Transconductance

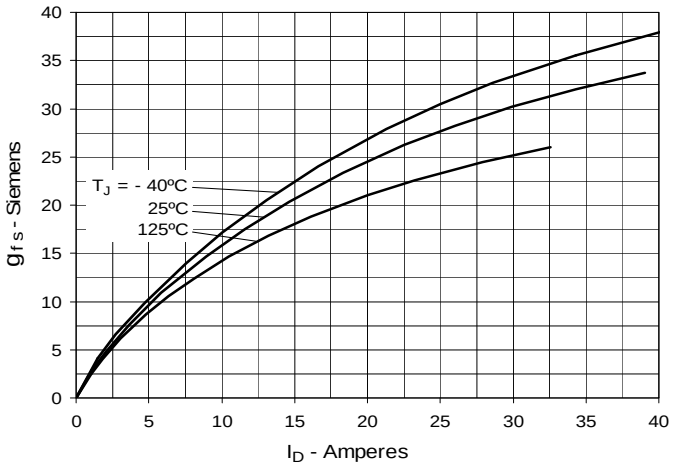


Fig. 9. Forward Voltage Drop of Intrinsic Diode

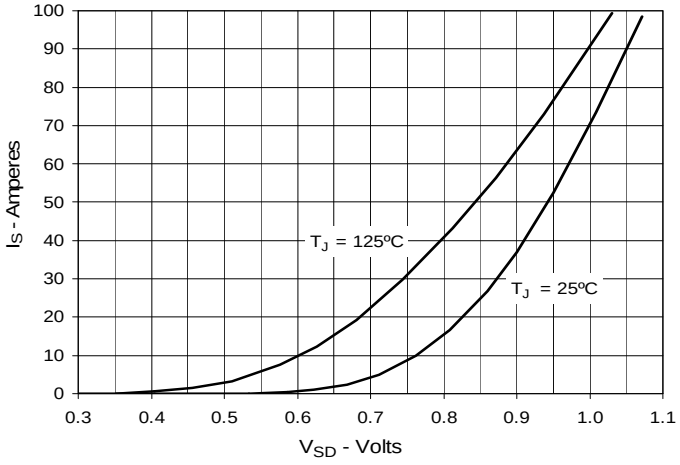


Fig. 10. Gate Charge

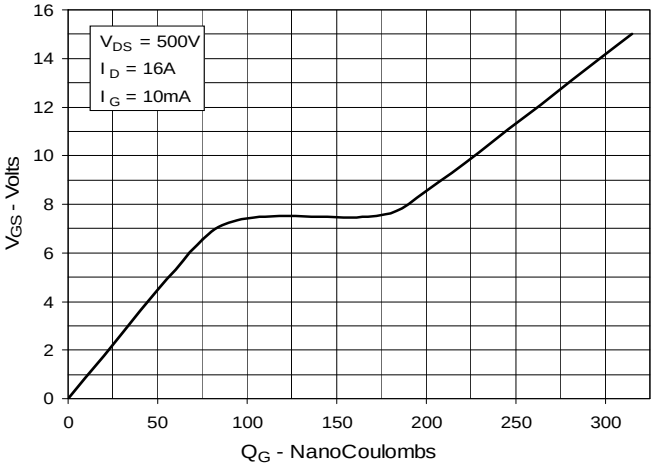


Fig. 11. Capacitance

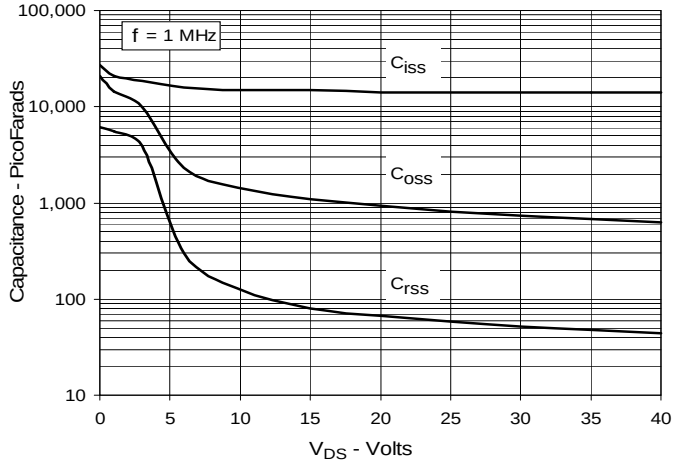
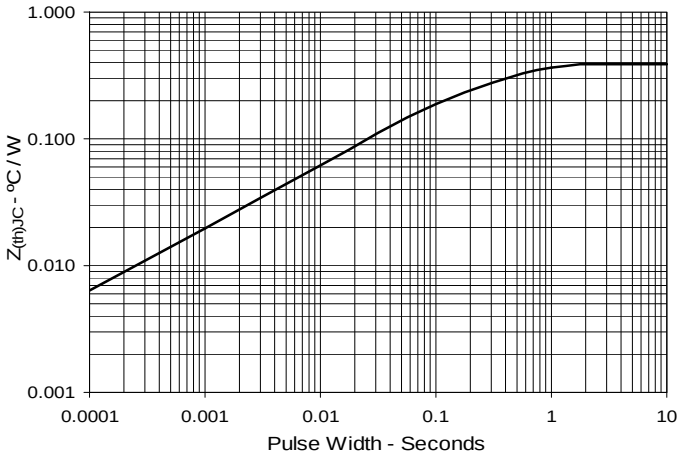


Fig. 12. Maximum Transient Thermal Impedance



IXYS reserves the right to change limits, test conditions, and dimensions.