

LTC2348 16-/18-Bit, Octal 200ksps SAR ADCs

DESCRIPTION

Demonstration circuit 2094A shows the proper way to drive the LTC[®]2348 family of ADCs. The LTC2348 are low noise, high speed, simultaneous sampling 16-/18-bit successive approximation register (SAR) ADCs. The following text refers to both parts in the family, the only difference being the number of bits. The LTC2348 has a flexible SoftSpan[™] interface that allows conversion-by-conversion control of the input voltage span on a per-channel basis. An internal 2.048V reference and 2X buffer simplify basic operation while an external reference can be used to increase the input range and the SNR of the ADC.

The DC2094 demonstrates the DC and AC performance of the LTC2348 in conjunction with the DC590/DC2026 and DC890 data collection boards. Use the DC590/DC2026 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The DC2094 is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. A suggested driver circuit for the analog inputs is also presented.

Design files for this circuit board including schematic and BOM are available at <http://www.linear.com/demo/DC2094A>

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ASSEMBLY OPTIONS

Table 1. DC2094A Assembly Options

ASSEMBLY VERSION	U1 PART NUMBER	MAX CONVERSION RATE (ksps)	NUMBER OF CHANNELS	NUMBER OF BITS	MAX CLK IN FREQUENCY (MHz)	CLK IN/ fs RATIO
DC2094A-A	LTC2348-18	200	8 Simultaneous	18	60	300
DC2094A-D	LTC2348-16	200	8 Simultaneous	16	60	300

DC2094A CONNECTION DIAGRAM

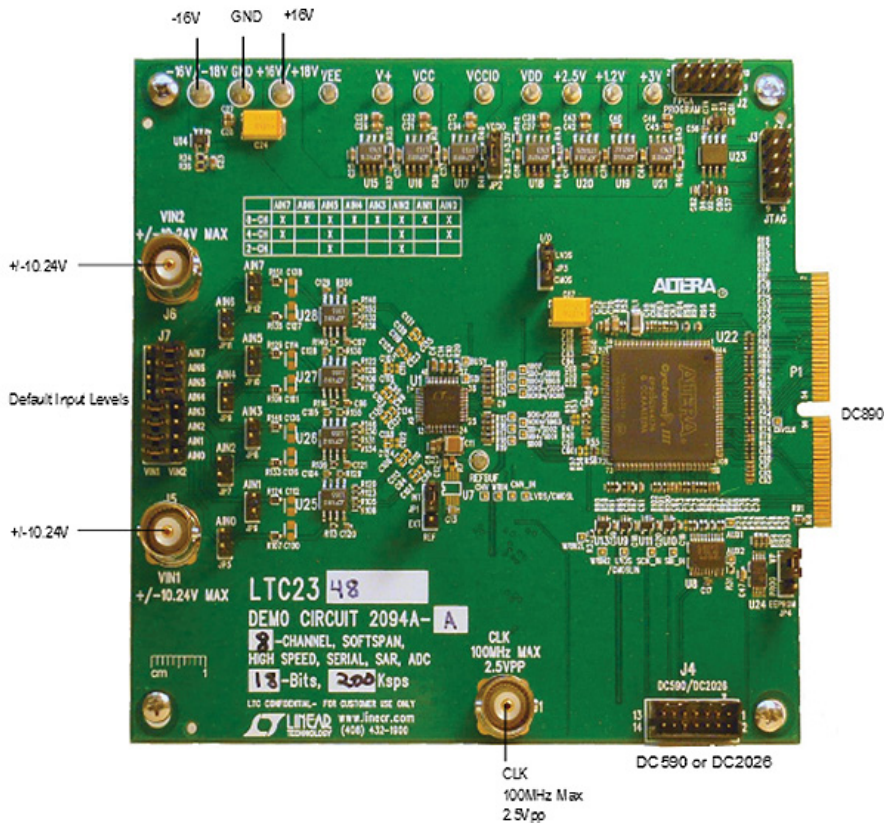


Figure 1. DC2094A Connection Diagram

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set to their default settings as described in the DC2094A Jumpers section of this manual. The default connections configure the ADC to use the onboard reference and regulators to generate all the required bias voltages. The analog inputs by default are DC coupled. Connect the DC2094A to a DC890 USB High Speed Data Collection Board using connector P1. Then, connect the DC890 to a host PC with a standard USB A/B cable. Apply $\pm 16V$ to the indicated terminals. Then apply a low jitter signal source to J5 and J6. Use J7 to route the signal sources of J5 and J6 to the desired AIN0-AIN7 inputs. Observe the recommended input voltage range for each analog input. Connect a low jitter $2.5V_{p-p}$ sine wave or square wave to connector J1. See Table 1 for the appropriate clock frequency. Note that J1 has a 50Ω termination resistor to ground.

Run the PScope™ software (Pscope.exe version K79 or later), which can be downloaded, from www.linear.com/designtools/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2094A and configure itself automatically.

Click the Collect button (see Figure 2) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC890 QUICK START PROCEDURE

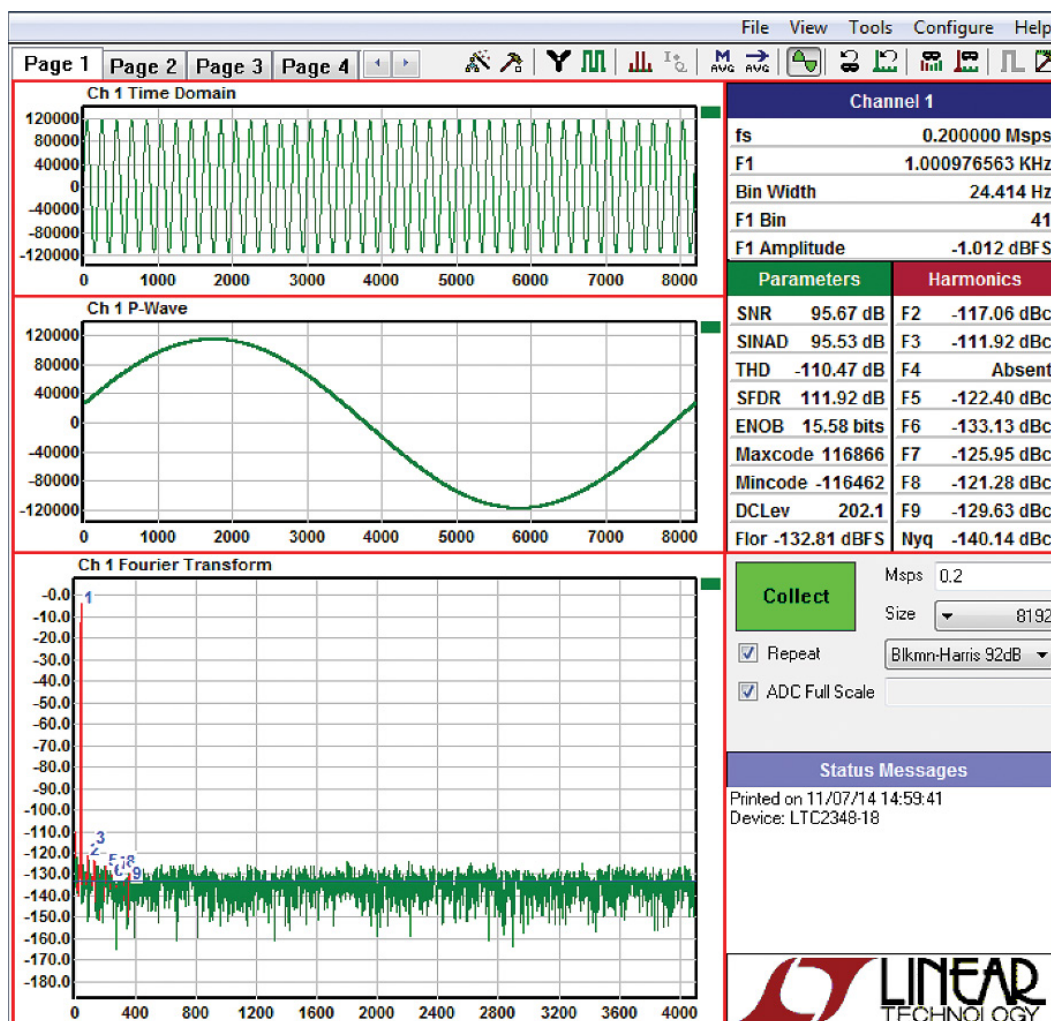


Figure 2. PScope Screen Shot

DC590/DC2026 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2094A, make sure that VCCIO (JP6 of the DC590, JP3 of the DC2026) of the DC590/DC2026 is set to 3.3V before connecting the DC590/DC2026 to the DC2094A.

To use the DC590/DC2026 with the DC2094A, it is necessary to apply $\pm 16V$ and ground to the $\pm 16V$ and GND terminals of the DC2094A. Connect the DC590/DC2026 to a host PC with a standard USB A/B cable. Connect the DC2094A to a DC590/DC2026 USB serial controller using the supplied 14-conductor ribbon cable. Apply a signal

source to J5 and J6. Use J7 to route the signal sources of J5 and J6 to the desired AIN0-AIN7 inputs. No Clock is required on J1 when using the DC590/DC2026. The clock signal is provided by the DC590/DC2026.

Run the QuikEval™ software (quikeval.exe version K105 or later), which is available from www.linear.com/design-tools/software. The correct control panel will be loaded automatically. Click the COLLECT button (Figure 6) to begin reading the ADC.

DC2094A SETUP

DC POWER

The DC2094A requires $\pm 16\text{VDC}$ and draws $+175\text{mA}$ – 12mA . Most of the supply current is consumed by the CPLD, op amps, regulators and discrete logic on the board. The $\pm 16\text{VDC}$ input voltage powers the ADC through LT1763 regulators, which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and opamps.

CLOCK SOURCE

You must provide a low jitter $2.5\text{V}_{\text{p-p}}$ sine or square wave to the clock input, J1. The clock input is AC coupled so the DC level of the clock signal is not important. A generator such as the Rohde & Schwarz SMB100A high speed clock source is recommended to drive the clock input. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore, it is recommended for lower sample rates to divide down a higher frequency clock to the desired sample rate. The ratio of clock frequency to conversion rate is shown in Table 1. If the clock input is to be driven with logic, it is recommended that the 49.9Ω termination resistor (R4) be removed. Driving R4 with discrete logic may result in slow rising edges. These slow rising edges may compromise the SNR of the converter in the presence of high-amplitude higher frequency input signals.

DATA OUTPUT

Parallel data output from this board (0V to 2.5V by default), if not connected to the DC890, can be acquired by a logic analyzer, and subsequently imported into a spreadsheet, or mathematical package depending on what form of digital

signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin 50 of P1 to latch the data. The data should be latched using the negative edge of this signal. The data output signal levels at P1 can also be increased to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving JP2 to the 3.3V position.

Reference

The default reference is the LTC2348 internal 4.096V reference. Alternatively, if a higher reference voltage is desired, the LTC6655-5 reference (U7) can be used by setting the REF jumper (JP1) to the EXT position and installing a 0Ω resistor in the R7 position. This should result in better SNR performance but may slightly degrade the THD performance of the LTC2348.

Analog Inputs

All eight inputs have the same driver circuitry. An example of the default driver circuit for the analog inputs of the LTC2348 on the DC2094A is shown in Figure 3. The circuit of Figure 3 provides a pseudo-differential output to Channel 2 and Channel 3 of the LTC2348 with a maximum $\pm 10.24\text{V}$ single-ended input voltage. Alternatively, the two single-ended channels shown can be combined to form a fully differential driver. In the circuit of Figure 3 this is done by removing R131 and changing R141 to 0Ω . At this point both AIN2 and AIN3 must be driven to $\pm 5.12\text{V}$ to achieve a full-scale input voltage for AIN2+ and AIN2– of the LTC2348. Changing R146 and R142 in a similar way would also allow AIN3+ and AIN3– of the LTC2348 to be driven fully differentially. Fully differential drive should provide a slight improvement in THD performance.

DC2094A SETUP

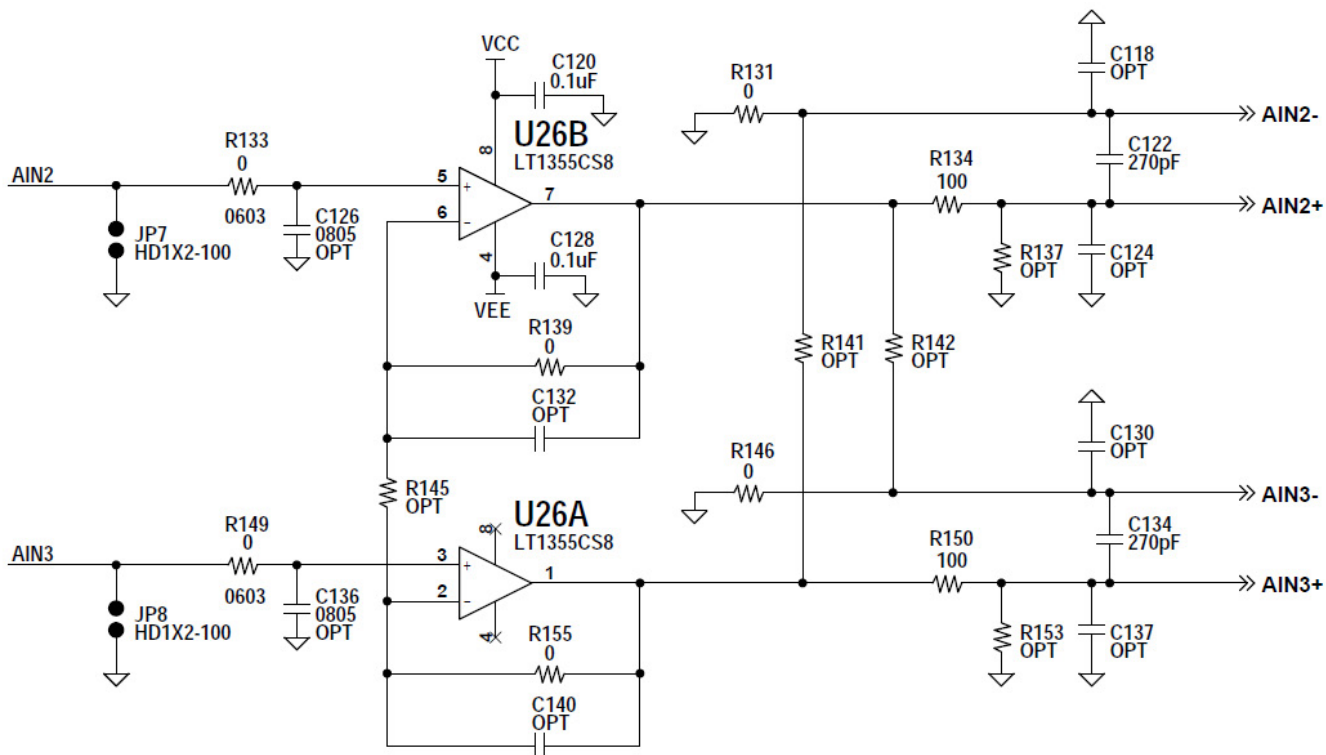


Figure 3. ±10.24V Pseudo-Differential DC Coupled Driver

DC890 DATA COLLECTION

For SINAD, THD or SNR testing a low noise, low distortion generator such as the B&K Type 1051 or Stanford Research SR1 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A is used to drive the clock input. This demo board is tested in house by attempting to duplicate the FFT plot shown in Typical Performance Characteristics section of the LTC2348 data sheet. This involves using a 60MHz clock source, along with a sinusoidal generator at a frequency of approximately 1kHz. The input signal level is approximately -1dBFS . A typical FFT obtained with DC2094A is shown in Figure 2. Note that to calculate the real SNR, the signal level ($F1$ amplitude = -1.012dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 2 this means that the actual SNR would be 96.68dB instead of the 95.67dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 96.5dB , which is fairly close to the typical number for this ADC.

To change the default settings for the LTC2348 in PScope, click on the Set Demo Bd Options button in the PScope tool bar shown in Figure 4. This will open the Configure Channels menu of Figure 5. In this menu it is possible to set the input signal range and gain compression setting for each channel. There is also a button to return PScope to the default DC2094A settings, which are optimized for the default hardware settings of the DC2094A.

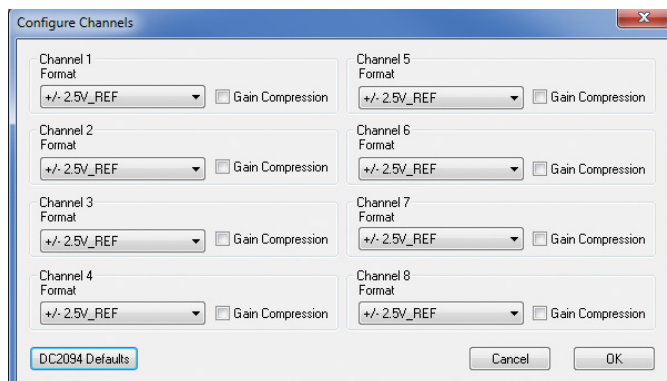


Figure 5. PScope Configuration Menu

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with an input frequency, that is a sub-multiple of the sample rate, and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and $N/2$. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the “leakage” or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

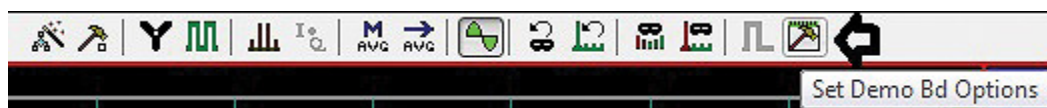


Figure 4. PScope Tool Bar

DC590/DC2026 DATA COLLECTION

Due to the relatively low and somewhat unpredictable sample rate of the DC590/DC2026, its usefulness is limited to noise measurement and data collection of slowly moving signals. A typical data capture and histogram are shown in Figure 6. To change the default settings for the LTC2348 in QuikEval click on the Channel Config. button. This will open the ConfigDialog menu of Figure 7. In this menu it is possible to set the input signal range and gain compression setting for each sequence. There is also a button to return QuikEval to the default DC2094A settings, which are optimized for the default hardware settings of the DC2094A.

LAYOUT

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2094A should be used as a guideline for placement, and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2348. A ground plane is necessary

to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

COMPONENT SELECTION

When driving a low noise, low distortion ADC such as the LTC2348, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self-heating. Because of their low voltage coefficients, to further reduce distortion NPO or silver mica capacitors should be used. Any buffer used to drive the LTC2348 should have low distortion, low noise and a fast settling time such as the LT1355.

DC590/DC2026 DATA COLLECTION

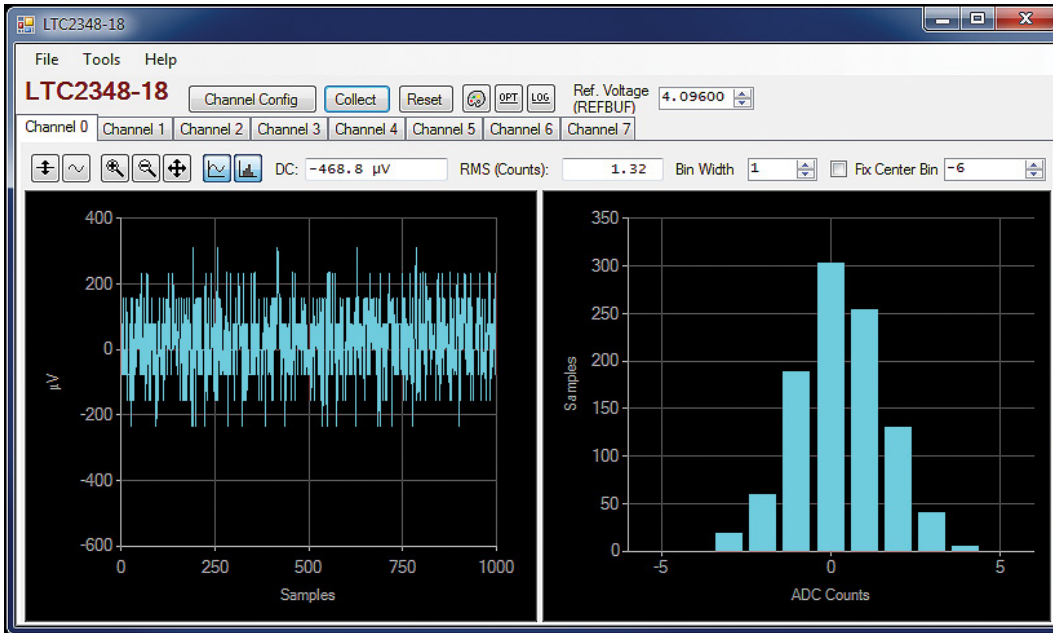


Figure 6. QuikEval Screen Shot

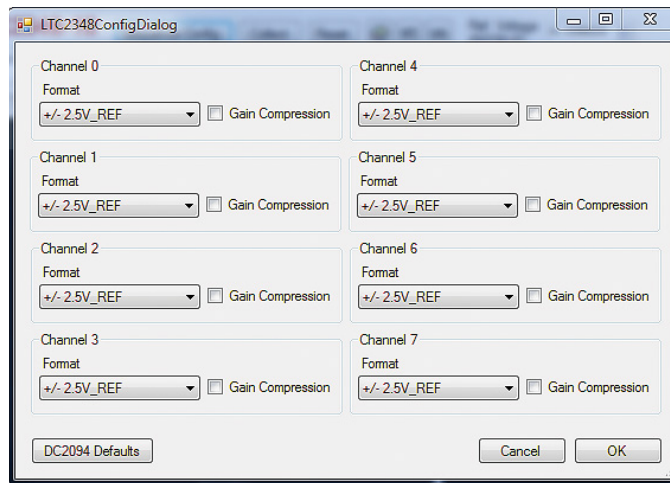


Figure 7. QuikEval Configuration Menu

DC2094A JUMPERS

DEFINITIONS

JP1 – REF selects INT or EXT reference for the ADC. The default setting is INT.

JP2 – VCCIO sets the output levels at P1 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890, which is the default setting. Use 3.3V to interface to the DC2026.

JP3 – I/O selects LVDS or CMOS logic levels. The default setting is CMOS. LVDS is for future use only.

JP4 – EEPROM is for factory use only. The default position is WP.

JP6 to JP12 – AIN0-AIN7 can be used to short individual AIN inputs to ground or can be used drive the individual AIN inputs. The default is to leave these open.

DC2094A CONNECTORS

DEFINITIONS

P1 – DC890 interface is used to communicate with the DC890 controller.

J1 – CLK provides the master clock for the DC2094A when interfaced to the DC890.

J2 – FPGA PROGRAM is used to program the FPGA. This is for factory use only.

J3 – JTAG is for factory use only.

J4 – DC590/DC2026 interface is used to communicate with the DC2026 Linduino controller or DC590.

J5 and J6 – Provide analog input voltages to AIN0-AIN7 of the ADC.

J7 – Routes the signals of J5 and J6 to AIN0-AIN7.

DEMO MANUAL DC2094A

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